What is claimed is:

1. A nonvolatile semiconductor memory comprising:

a control section;

a memory array section; and

a voltage generation section,

said memory array section comprising:

a first semiconductor region;

a second semiconductor region on the first semiconductor region; and

a memory cell section formed on the second semiconductor region, and wherein

said control section outputs a control signal instructing the voltage generation section to generate a voltage applied to said second semiconductor region when or before receiving an access instruction from an outside indicating that it is necessary to charge said second semiconductor region; and

said control section outputs a control signal to said voltage generation section to discharge said second semiconductor region when instructed from the outside to discharge said second semiconductor region.

2. A nonvolatile semiconductor memory comprising:

a control section;

a memory array section; and

a voltage generation section,

said memory array section comprising:

a first semiconductor region;

a second semiconductor region formed on the first semiconductor region;

a memory cell section formed on the second semiconductor region, and wherein

said control section is capable of receiving a first operation instruction and a second operation instruction from an outside;

said control section instructs said voltage generation section to generate a voltage applied to said second semiconductor region to charge said second semiconductor region when receiving said first operation instruction; and

said control section instructs said voltage generation section to discharge said second semiconductor region when receiving said second operation instruction.

3. An information processing apparatus comprising:

a central processing unit; and

a nonvolatile semiconductor memory, both of said central processing unit and said nonvolatile semiconductor memory being formed on one semiconductor substrate, wherein

said nonvolatile semiconductor memory comprises a memory array section and a voltage generation section, and carries out operations including a first operation and a second operation in accordance with a control signal from said central processing unit;

said memory array section has a first semiconductor region and a memory cell section formed on said semiconductor substrate, the memory cell section storing data in the first

semiconductor region;

said central processing unit comprises a register section storing states;

said central processing unit instructs said nonvolatile semiconductor memory to generate a voltage for charging said first semiconductor region during first time if said first operation is indicated to said nonvolatile semiconductor memory and said register section shows a first state;

said central processing unit instructs said nonvolatile semiconductor memory to generate a voltage for charging said first semiconductor region during second time if said second operation is indicated to said nonvolatile semiconductor memory and said register section shows a second state; and

said central processing unit instructs said nonvolatile semiconductor memory to discharge said first semiconductor region to turn said register section into the first state if said second operation is indicated to said nonvolatile semiconductor memory.

4. A nonvolatile semiconductor memory system comprising:

a control device; and

at least one nonvolatile semiconductor memory, wherein

said control section comprises an interface section interfacing said nonvolatile semiconductor memory system with an outside, said control section receiving an instruction from the outside to carry out a first operation and a second operation, and selecting a predetermined nonvolatile semiconductor memory in accordance with an operation

instruction, outputting a first operation signal to the selected nonvolatile semiconductor memory in accordance with said first operation, and sequentially outputting a second operation signal and a third operation signal in accordance with the second operation,

said at least one nonvolatile semiconductor memory comprises a control section, a memory array section, and a voltage generation section;

said memory array section comprises a first semiconductor region, a second semiconductor region formed on the first semiconductor region, and a memory cell section formed on the second semiconductor region;

said control section of said nonvolatile semiconductor memory instructs said voltage generation section to generate a voltage for charging said second semiconductor region in accordance with said first operation signal, and carries out a predetermined operation in accordance with the first operation signal when charging of said second semiconductor region is completed;

said control section carries out a discharge operation for discharging said second semiconductor region in response to said second operation signal; and

said control section carries out a predetermined operation in accordance with said third operation signal, in response to said third operation signal.

5. A nonvolatile semiconductor memory system comprising:

a control section; and

at least one nonvolatile semiconductor memory, wherein

said control section comprises an interface section interfacing said nonvolatile memory system with an outside, said control section receiving an instruction from the outside through said interface section to carry out a first operation and a second operation, selecting a predetermined nonvolatile semiconductor memory in accordance with an operation instruction, sequentially outputting a first operation signal and a second operation signal to the selected nonvolatile semiconductor memory in accordance with said first operation, and outputting a third operation signal in accordance with said second operation;

said at least one nonvolatile semiconductor memory comprises a control section, a memory array section, and a voltage generation section;

said memory array section comprises a first semiconductor region, a second semiconductor region formed on the first semiconductor region, and a memory cell section formed on the second semiconductor region;

said control section of said nonvolatile semiconductor memory instructs said voltage generation section to generate a voltage for charging said second semiconductor region in accordance with said first operation;

said control section carries out a predetermined operation in accordance with said second operation signal, in response to said second operation signal; and

said control section carries out a predetermined

operation in accordance with the said third operation signal, in response to said third operation signal.

6. A nonvolatile semiconductor memory comprising:

(a) a memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in a first semiconductor region in a semiconductor substrate; a charge accumulation layer formed on a region between said second semiconductor regions for the source and the drain, through a gate insulating film; and a control electrode provided on said charge accumulation layer through an insulating film;

(b) a third semiconductor region formed between said first semiconductor region and the semiconductor substrate;

(c) first voltage application means for applying a voltage to said control electrode;

(d) a second voltage application means for applying a voltage to said first semiconductor region; and

(e) a third voltage application means for applying a voltage to said third semiconductor region.

7. A nonvolatile semiconductor memory according to claim 6, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation layer to be

pulled out into said first semiconductor region.

8. A nonvolatile semiconductor memory according to claim 6, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region by a tunnel phenomenon.

9. A nonvolatile semiconductor memory according to claim 6, wherein

a first voltage is applied to the control section of said nonvolatile semiconductor memory, a second voltage is applied to said first semiconductor region, and a third voltage is applied to said third semiconductor region; and

said third voltage is higher than said second voltage.

10. A nonvolatile semiconductor memory according to claim 6, wherein

said nonvolatile semiconductor memory applies a first voltage to said control electrode, and applies a second voltage to said first semiconductor region, thereby pulling out electrons accumulated in said charge accumulation layer into said first semiconductor region, to thereby allow data to be electrically deleted.

11. A nonvolatile semiconductor memory according to claim 6,

wherein

said nonvolatile semiconductor memory comprises a plurality of memory cell groups each having a plurality of said memory cells formed therein, and the memory cells in each memory cell group are formed above a non-separated third semiconductor region.

12. A nonvolatile semiconductor memory according to claim 6, wherein

said nonvolatile semiconductor memory comprises a plurality of memory cell groups each having a plurality of said memory cells formed therein, and the memory cells in each memory cell group are formed above a third semiconductor region separated at intervals of units of a predetermined number of the memory cells.

13. A nonvolatile semiconductor memory according to claim 6, wherein

said nonvolatile semiconductor memory comprises a plurality of first memory cell groups each having a plurality of said memory cells in units of a first predetermined number of the memory cells; and a plurality of second memory cell groups each having said memory cells in units of a second predetermined number of the memory cells, the second predetermined number being higher than said first predetermined number;

the memory cells in said plurality of first memory cell groups are formed above a third semiconductor region separated at intervals of units of a third predetermined number of the

memory cells; and

the memory cells in said plurality of second memory cell groups are formed above the third semiconductor region separated at intervals of units of a fourth predetermined number of the memory cells, the fourth predetermined number being higher than the third predetermined number.

14. A nonvolatile semiconductor memory according to claim 6, wherein

said nonvolatile semiconductor memory further comprises means for determining a threshold voltage of said memory cell;

a first voltage is applied to said control electrode and a second voltage is applied to said first semiconductor region during a first period, thereby allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region;

the threshold voltage of said memory cell is determined in a second period following said first period;

if it is determined that the threshold voltage of said memory cell is higher than a predetermined threshold voltage, the first voltage is applied to said control electrode and the second voltage is applied to said first semiconductor region in a third period following said second period, thereby allowing the electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region.

15. A nonvolatile semiconductor memory according to claim 14, wherein

a third voltage is applied to said third semiconductor

region during said first to third periods.

16. A data deletion method for a nonvolatile semiconductor memory, the nonvolatile semiconductor memory comprising:

a memory cell comprising: second semiconductor regions for a source and a drain, respectively, formed in a first semiconductor region in a semiconductor substrate; a charge accumulation layer formed on a region between said second semiconductor regions for the source and the drain through a gate insulating film; and a control electrode provided on said charge accumulation layer through an insulating film; and

a third semiconductor region formed between said first semiconductor region and the semiconductor substrate, wherein

the data deletion method is performed to delete data accumulated in said charge accumulation layer by applying a first voltage to said control electrode and a second voltage to said first semiconductor region, and by pulling out electrons accumulated in said charge accumulation layer into said first semiconductor region based on a potential difference between said first voltage and said second voltage, and wherein

a third voltage supplied from voltage supply means different from voltage supply means supplying said second voltage, is applied to said third semiconductor region while the first voltage is applied to said control electrode and the second voltage is applied to said first semiconductor region.

17. A data deletion method for a nonvolatile semiconductor memory, according to claim 16, wherein

said third voltage is higher than said second voltage.

18. A data deletion method for a nonvolatile semiconductor memory, the nonvolatile semiconductor memory comprising:

a memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in a first semiconductor region in a semiconductor substrate; a charge accumulation layer formed on a region between said second semiconductor regions for the source and the drain through a gate insulating film; and a control electrode provided on said charge accumulation layer through an insulating film; and

a third semiconductor region formed between said first semiconductor region and the semiconductor substrate, wherein

the data deletion method comprising the steps of:

applying a first voltage to said control electrode, applying a second voltage to said first semiconductor region, and pulling out electrons accumulated in said charge accumulation layer into said first semiconductor region based on a potential difference between said first voltage and said second voltage in a first period;

determining a threshold voltage of said memory cell in a second period following said first period; and

applying the first voltage to said control electrode, applying the second voltage to said first semiconductor region and thereby pulling out the electrons accumulated in said charge accumulation layer into said first semiconductor region in a third period following said second period if the threshold voltage of said memory cell is higher than a

predetermined threshold voltage, and wherein

a third voltage is applied to said third semiconductor region during said first to third periods.

19. A data deletion method for a nonvolatile semiconductor memory, according to claim 18, wherein

said third voltage is higher than said second voltage.

20. A nonvolatile semiconductor memory comprising:

(a) a memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in a first semiconductor region in a semiconductor substrate; a charge accumulation layer formed on a region between said second semiconductor regions for the source and the drain through a gate insulating film; and a control electrode provided on said charge accumulation layer through an insulating film;

(b) a third semiconductor region (NiSO) formed between said first semiconductor region and the semiconductor substrate;

(c) first means for applying a voltage to said control electrode;

(d) second means for applying a voltage to said first semiconductor region; and

(e) third means for prohibiting a voltage from being applied to said third semiconductor region.

21. A nonvolatile semiconductor memory according to claim 20, wherein

a first voltage is applied to the control electrode of

said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region.

22. A nonvolatile semiconductor memory according to claim 20, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region by a tunnel phenomenon.

23. A nonvolatile semiconductor memory according to claim 20, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory by said first means; a second voltage is applied to said first semiconductor region by said second means; and said third semiconductor region is maintained in a floating state by said third means.

24. A nonvolatile semiconductor memory according to claim 20, wherein

said nonvolatile semiconductor memory applies a first voltage to said control electrode, and applies a second

voltage to said first semiconductor region, thereby pulling out electrons accumulated in said charge accumulation layer into said first semiconductor region, to thereby allow data to be electrically deleted.

25. A nonvolatile semiconductor memory according to claim 20, wherein

said nonvolatile semiconductor memory comprises a plurality of memory cell groups each having a plurality of said memory cells formed therein, and the memory cells in each memory cell group are formed above a non-separated third semiconductor region.

26. A nonvolatile semiconductor memory according to claim 20, wherein

said nonvolatile semiconductor memory comprises a plurality of memory cell groups each having a plurality of said memory cells formed therein, and the memory cells in each memory cell group are formed above a third semiconductor region separated at intervals of units of a predetermined number of the memory cells.

27. A nonvolatile semiconductor memory according to claim 20, wherein

said nonvolatile semiconductor memory comprises a plurality of first memory cell groups each having a plurality of said memory cells in units of a first predetermined number of the memory cells; and a plurality of second memory cell groups each having said memory cells in units of a second predetermined number of the memory cells, the second

predetermined number being higher than said first predetermined number;

the memory cells in said plurality of first memory cell groups are formed above a third semiconductor region separated at intervals of units of a third predetermined number of the memory cells; and

said first semiconductor region having the memory cells in said plurality of second memory cell groups formed therein is formed in the third semiconductor region separated at intervals of units of a fourth predetermined number of the memory cells, the fourth predetermined number being higher than the third predetermined number.

28. A nonvolatile semiconductor memory according to claim 20, wherein

said nonvolatile semiconductor memory further comprises means for determining a threshold voltage of said memory cell;

a first voltage is applied to said control electrode and a second voltage is applied to said first semiconductor region in a first period, thereby allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region;

the threshold voltage of said memory cell is determined in a second period following said first period;

if it is determined that the threshold voltage of said memory cell is higher than a predetermined threshold voltage, the first voltage is applied to said control electrode and the second voltage is applied to said first semiconductor region

in a third period following said second period, thereby allowing the electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region.

29. A nonvolatile semiconductor memory according to claim 28, wherein

said third semiconductor region is maintained in a floating state during said first to third periods.

30. A data deletion method for a nonvolatile semiconductor memory, the nonvolatile semiconductor memory comprising:

a memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in a first semiconductor region in a semiconductor substrate; a charge accumulation layer formed on a region between said second semiconductor regions for the source and the drain through a gate insulating film; and a control electrode provided on said charge accumulation layer through an insulating film; and

a third semiconductor region formed between said first semiconductor region and the semiconductor substrate, wherein

the data deletion method is performed to delete data accumulated in said charge accumulation layer by applying a first voltage to said control electrode and a second voltage to said first semiconductor region, and by pulling out electrons accumulated in said charge accumulation layer into said first semiconductor region based on a potential difference between said first voltage and said second voltage, and wherein

said third semiconductor region is maintained in a

floating state while the first voltage is applied to said control electrode and the second voltage is applied to said first semiconductor region.

31. A data deletion method for a nonvolatile semiconductor memory, the nonvolatile semiconductor memory comprising:

a memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in a first semiconductor region in a semiconductor substrate; a charge accumulation layer formed on a region between said second semiconductor regions for the source and the drain through a gate insulating film; and a control electrode provided on said charge accumulation layer through an insulating film; and

a third semiconductor region formed between said first semiconductor region and the semiconductor substrate, wherein

the data deletion method comprises the steps of:

applying a first voltage to said control electrode, applying a second voltage to said first semiconductor region, and pulling out electrons accumulated in said charge accumulation layer into said first semiconductor region based on a potential difference between said first voltage and said second voltage in a first period;

determining a threshold voltage of said memory cell in a second period following said first period; and

applying the first voltage to said control electrode, applying the second voltage to said first semiconductor region and thereby pulling out the electrons accumulated in said charge accumulation layer, into said first semiconductor

region in a third period following said second period if the threshold voltage of said memory cell is higher than a predetermined threshold voltage, and wherein

said third semiconductor region is maintained in a floating state during said first to third periods.

32. A nonvolatile semiconductor memory comprising:

(a) a plurality of memory cell groups each having a plurality of memory cells formed on a main surface of a first semiconductor region in a semiconductor substrate, each memory cell comprising second semiconductor regions for a source and a drain, respectively, formed in said first semiconductor region; a charge accumulation layer formed on a region between the second semiconductor regions for the source and the drain through a gate insulating film; and a control electrode provided on said charge accumulation layer through an insulating film;

(b) a third semiconductor region formed between said first semiconductor region and the semiconductor substrate;

(c) first voltage application means for applying a voltage to said control electrode; and

(d) second voltage application means for applying a voltage to said first semiconductor region and said third semiconductor region, respectively, wherein

said third semiconductor region is separated at intervals of units of a predetermined number of the memory cells in the plurality of memory cell groups.

33. A nonvolatile semiconductor memory according to claim

32, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region and said third semiconductor region, respectively; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region.

34. A nonvolatile semiconductor memory according to claim 32, wherein

a first voltage is applied to the control electrode of said nonvolatile semiconductor memory, and a second voltage is applied to said first semiconductor region and said third semiconductor region, respectively; and

a potential difference between said first voltage and said second voltage corresponds to a voltage allowing electrons accumulated in said charge accumulation layer to be pulled out into said first semiconductor region by a tunnel phenomenon.

35. A nonvolatile semiconductor memory according to claim 32, wherein

said plurality of memory cell groups comprise a plurality of first memory cell groups each having a plurality of said memory cells in units of a first predetermined number of the memory cells; and a plurality of second memory cell groups each having said memory cells in units of a second

predetermined number of the memory cells, the second predetermined number being higher than said first predetermined number;

the memory cells in said plurality of first memory cell groups are formed above a third semiconductor region separated at intervals of units of a third predetermined number of the memory cells; and

the memory cells in said plurality of second memory cell groups are formed above the third semiconductor region separated at intervals of units of a fourth predetermined number of the memory cells, the fourth predetermined number being higher than the third predetermined number.

36. A nonvolatile semiconductor memory according to claim 1, wherein

said memory cell section comprises a plurality of memory cells, and

each of the plurality of memory cells comprises a channel region; a first region and a second region formed in the channel region; a charge accumulation region formed on the channel region; and a control gate region formed on the charge accumulation region.

37. An information processing apparatus according to claim 3, wherein

said memory cell section comprises a plurality of memory cells, and

each of the plurality of memory cells comprises a channel region; a first region and a second region formed in

the channel region; a charge accumulation region formed on the channel region; and a control gate region formed on the charge accumulation region.

38. A nonvolatile semiconductor memory system according to claim 4, wherein

said memory cell section comprises a plurality of memory cells, and

each of the plurality of memory cells comprises a channel region; a first region and a second region formed in the channel region; a charge accumulation region formed on the channel region; and a control gate region formed on the charge accumulation region.